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EXAMINER

TORRES, JOSEPH D

ART UNIT	PAPER NUMBER
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2133

DATE MAILED: 08/19/2003

12

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/368,918

Applicant(s)

TRABER ET AL.

Examiner

Joseph D. Torres

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 29 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 15-21 is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☒ Claim(s) 4-10 and 13 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 19 August 2002 is: a) ☒ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Drawings*

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 19 August 2002 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

### *Specification*

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that **the abstract not exceed 150 words in length** since the space provided for the abstract on the computer tape used by the printer is limited. The **form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided**. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The abstract of the disclosure is objected to because **the abstract exceeds 150 words** in length and because of **form and legal phraseology** often used in patent claims, such as "means" and **"said," is used**. Correction is required. See MPEP § 608.01(b).

***Claim Objections***

3. Claims 4-10 and 13 are objected to because of the following informalities: Claim 4 and 13 recite the language "adapted to". MPEP § 2106 (II) C states language that suggests or makes optional but does not require steps to be performed or does not limit a claim to a particular structure does not limit the scope of a claim or claim limitation. The phrases starting "adapted to ..." in claims 4 and 13 fail to limit the scope of the claims. Claims 5-10 depend from claim 4, hence inherit the deficiencies of claim 4. Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 4-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 1 recites the following limitation, "a first stage scan enabling component coupled to said scan test enable trigger sensing component, said first stage scan enabling component adapted to track logical values of the trigger signal from **a first stage**" [Emphasis Added]. Nowhere does the Applicant teach a first scan element tracking a signal that it receives from itself. Claim 1 recites the following limitation, "a

second stage scan enabling component coupled to said scan test enable trigger sensing component, said second stage scan enabling component adapted to track logical values of the trigger signal from a second stage" [Emphasis Added]. Nowhere does the Applicant teach a second scan element tracking a signal that it receives from itself.

Claims 5-10 depend from claim 4, hence inherit the deficiencies of claim 4

### ***Response to Arguments***

5. Applicant's arguments with respect to previously examined claims 1-14 filed 29 July 2003 have been fully considered but they are not persuasive.

The Applicant contends, "Li does not teach that the output of OR gate 94 provides any notification to "flip flops 91" [Fig 4A does not show any connection of the OR gate 94 output to "flip flops 91"J and does not teach the "flip flops 91"] doing anything based upon the output of OR gate 94. Applicants respectfully assert that "flip flops 91" of Li can not do anything based upon notification from OR gate 94 because OR gate 94 does not provide any information to "flip flops 91"". The Examiner disagrees and asserts that nowhere does claim 1 teach a notification to a flip-flop, hence does not see how the argument is relevant to the Applicants current claim language

The Applicant contends, "to the extent the Li reference may teach that the use of scan test mode signal for enabling a scan test it does not teach a trigger signal providing an

indication to begin a scan test enable signal assertion". The Examiner disagrees and asserts that the Authoritative Dictionary of IEEE Standard Terms defines trigger as a signal to start an action. The scan test enable signal is a signal used to start an action, hence is a trigger signal. Furthermore the scan test enable "trigger" signal 53 in Figure 3 of Li provides an assertion or deassertion notification to enable MUX scanning according to the timing chart of Figure 5 in Li.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Li, Hehching Harry (US 6023778 A).

35 U.S.C. 102(e) rejection of claim 1.

Li teaches an automatic scan test enable signal assertion system (see Figures 3 & 4B; col. 3, lines 55-67 and col. 4, lines 21-31, Li) comprising: a scan test enable trigger sensing component (see OR circuit 94, Li) for providing an assertion or deassertion notification when logical values of a trigger signal (scan mode signals received via mode

input 53 are trigger signals, col. 3, lines 59-58, Li) captured during multiple stages (see 97, 98 and 100 in Figure 4B, Li) provide an indication to begin a scan test enable signal assertion or deassertion (see 55 in Figure 4B and col. 4, lines 1-2, Li; Note: mode output makes available the scan mode signal to the Mux Scan Flip-Flops to enable the scan test); and a staging component (see 91 in Figure 4B, Li) coupled to said scan test enable trigger sensing component (see OR circuit 94, Li), said staging component adapted to advance said logical values of said trigger signal through a plurality of stages in accordance with a progression signal (clock signal 52, in Figures 3 & 4B in Li, is a progression signal) and issue an asserted or deasserted scan test enable signal based upon said assertion or deassertion notification from said scan test enable trigger sensing component (see Abstract, Li).

35 U.S.C. 102(e) rejection of claim 3.

Figure 3 is an embodiment of a test circuit (col. 3, lines 55-60, Li).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
  2. Ascertaining the differences between the prior art and the claims at issue.
  3. Resolving the level of ordinary skill in the pertinent art.
  4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
7. Claims 2 and 4-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li, Hehching Harry (US 6023778 A).

35 U.S.C. 103(a) rejection of claim 2.

Li substantially teaches the claimed invention described in claim 1 (as rejected above). However Li does not explicitly teach the specific use of a PCI reset signal as a trigger signal.

The Examiner would like to point out that a reset signal is a binary signal as expected from the scan mode pad 50 in Figure 3, hence use of a reset signal does not deviate from the scope or the intent of the teachings in Li, since a reset signal is a binary signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Li by including use of a PCI reset signal as a trigger signal. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a PCI reset signal as a trigger signal would have provided a a binary means as taught in the Lee patent for enabling the test.



35 U.S.C. 103(a) rejection of claims 4 and 7.

The Examiner would like to point out that the Li teaches two stages to delay the test enable signal. Expanding to a specific embodiment with a means for delaying the test enable signal with three stages does not deviate from the scope or the intent of the teachings in Li, since one of ordinary skill in the art at the time the invention was made would have known that a third stage would add an additional clock delay. The Examiner would also like to point out that given the clocking requirements of Figure 5 in Li, one of ordinary skill in the art at the time the invention was made would have known how to design a circuit to implement the requirements. One ordinary skill in the art at the time the invention was made would also have known how to implement an embodiment with a three-cycle clock delay.

35 U.S.C. 103(a) rejection of claim 5.

See Rejection to claim 2, above.

35 U.S.C. 103(a) rejection of claim 6.

See 201 and 204 in Figure 5, Li.

35 U.S.C. 103(a) rejection of claims 8 and 9.

See Rejection to claim 5 and Figure 5 in Li.

35 U.S.C. 103(a) rejection of claim 10.

A particular embodiment for the test activation system does not deviate from the scope or the teachings of the Li patent (see rejections to claims 1-9, above).

35 U.S.C. 103(a) rejection of claim 11.

Li teaches an automatic scan test enable signal activation system comprising: a scan test enable signal assertion system (see Figures 3 & 4B; col. 3, lines 55-67 and col. 4, lines 21-31, Li) adapted to automatically assert or deassert the scan test enable signal in response to transitions in a trigger signal and stage progression signal (scan mode signals received via mode input 53 are trigger signals, col. 3, lines 59-58, Li; and clock signal 52, in Figures 3 & 4B in Li, is a progression signal); a multiplexer (MUX) coupled to said automatic scan test enable signal assertion system (see MUX's 62, 68, 75, 81 and 87 in Figure 3 in Li), said multiplexer is adapted to facilitate transmission of signals depending upon the assertion of a scan test enable signal (see delay Circuit 54 and MUX's 62, 68, 75, 81 and 87 in Figure 3 in Li); a functional component coupled to said multiplexer (see Integrated Circuit Logic 70 in figure 3 of Li), said functional component is adapted to perform normal operations of an ASIC or printed circuit board (col. 1, lines 9-11, Li); an input port coupled to said functional component (see 72 in Figure 3, Li), said input port is adapted to function as input connections that communicate signals to said ASIC or said printed circuit board; an MUX Scan Flop 75 gate coupled to said input port, said MUX Scan Flop 72 gate is adapted to capture information from said input port; and a test data output port (see 72 in Figure 3, Li) coupled to said multiplexer, said test

data output port adapted to communicate test data off of the Integrated Circuit 70 (see 76 in Figure 3, Li).

However Li does not explicitly teach the specific use of a NAND gate coupled to said input port.

The Examiner would like to point out that the NAND gate serves the purpose of capturing data to be inputted into a functional logic component of an integrated circuit.

The MUX's 62 and 68 in LI serve the purpose of capturing data to be inputted into a functional logic component of an integrated circuit hence using a NAND gate in place of the MUX in Fig. 3 of Li does not deviate from the scope or the intent of the teachings in the Li patent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Li by including use of a NAND gate coupled to said input port. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a NAND gate coupled to said input port would have provided a means for capturing data to be inputted into a functional logic component of an integrated circuit.

35 U.S.C. 103(a) rejection of claim 12.

The MUX's 62 and 68 in LI serve the purpose of capturing data to be inputted into a functional logic component of an integrated circuit hence using a NAND gate in place of

the MUX in Fig. 3 of Li does not deviate from the scope or the intent of the teachings in the Li patent.

35 U.S.C. 103(a) rejection of claim 13.

See Figure 3 in Li and rejections to claims 11 and 12, above.

35 U.S.C. 103(a) rejection of claim 14.

See MUX F-F 75 in Figure 3 of Li.

### ***Allowable Subject Matter***

8. Claims 15-21 are allowed.

### ***Conclusion***

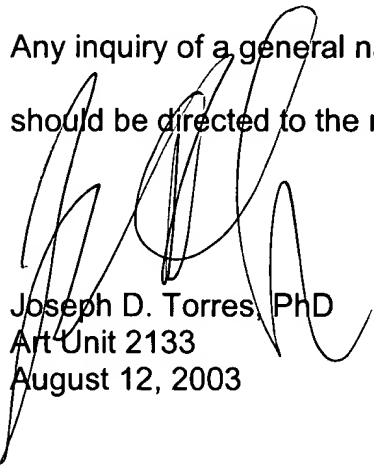
9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Slemmer, William C. (US 5072137 A) teaches semiconductor memories, and is specifically directed to the entry into special test modes for such memories.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.



Joseph D. Torres, PhD  
Art Unit 2133  
August 12, 2003